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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/733,352	12/12/2003	Shunpei Yamazaki	0756-7227	7478

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EXAMINER	
ISAAC, STANETTA D	
ART UNIT	**PAPER NUMBER**
2812	

DATE MAILED: 04/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/733,352	YAMAZAKI ET AL.	
	Examiner	Art Unit	
	Stanetta D. Isaac	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *10-21 and 30-40* is/are allowed.

6)☒ Claim(s) *1-9 and 22-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement (IDS) filed on 01/28/02 has been considered by the examiner.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-9 and 22-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ueda et al. US Patent 6,337,259 in view of Gotou et al. US Patent 6,436,745.

4. Pertaining to claims 1 and 22,Ueda discloses the semiconductor process substantially as claimed. See **FIGS. 1-7F** where Ueda teaches a process for producing a semiconductor device, comprising: forming a first semiconductor film having an amorphous structure; adding an element for promoting crystallization to the first semiconductor film having the amorphous structure; conducting a first heat treatment to form a first semiconductor film having a crystal structure.

5. However pertaining to claims 1-3 and 22, Ueda fails the process of forming a second semiconductor film (formed by sputtering and/or CVD) containing a rare gas element over the first semiconductor film having the crystal structure; conducting a second heat treatment to segregate the element for promoting crystallization into the second semiconductor film; and removing the second semiconductor film. See **FIGS. 1A-1G**, where Gotou teaches the above

process. In view of Gotou it would have been obvious to one of ordinary skill to incorporate Gotou into Ueda semiconductor process because a gettering process is conducted using the second silicon directly formed on the whole surface of the first silicon film instead of using parts of the first silicon film in addition, a catalytic metal element is used to promote crystallization of silicon. (See **col. 6 lines 27-67; col. 7 line 45**)

6. Pertaining to claims 4 and 24, Ueda teaches a process according to claims 1 and 22, wherein the first heat treatment is conducted by radiation from one or more selected from halogen lamp, a metal halide lamp, a xenon arc lamp, a carbon arc lamp, a high-pressure sodium lamp, or a high-pressure mercury lamp.

7. Pertaining to claims 5 and 25, Ueda teaches a process according to claims 1 and 22, wherein the first heat treatment is conducted by furnace annealing using an electrical heating furnace.

8. Pertaining to claims 6 and 26, Ueda teaches a process according to claims 1 and 22, wherein the second heat treatment is conducted by radiation from one or more selected from a halogen lamp, a metal halide lamp, a xenon arc lamp, a carbon arc lamp, a high-pressure sodium lamp, or a high-pressure mercury lamp.

9. Pertaining to claims 7 and 27, Ueda teaches a process according to claims 1 and 22, wherein the second heat treatment is conducted by furnace annealing using an electrical heating furnace.

10. Pertaining to claims 8 and 28, Ueda teaches a process according to claims 1 and 22, wherein the rare gas element is one or selected from He, Ne, Ar, Kr, and Xe.

11. Pertaining to claims 9 and 29, Ueda teaches a process according to claims 1 and 22, wherein the element for promoting crystallization is one or more selected from Fe, Ni, Co, Ru, Rh, Pd, Os, Ir, Pt, Cu, and Au.

12. Pertaining to claim 23, Ueda teaches a process according to claim 22, wherein the rare gas element is added by ion implantation or ion doping.

Allowable Subject Matter

13. Claims 10-21 and 30-40 are allowed.

14. The following is an examiner's statement of reasons for allowance: Applicant's independent claims 10 and 30 are allowed over the prior art of record because none teach or render obvious a process for producing a semiconductor device, comprising forming a second semiconductor film containing a rare gas element over the barrier layer. See in combination **Ueda et al.** US patent **6,337,259** and **Gotou et al.** US Patent **6,436,745** teaches the process for producing a semiconductor device however, fails separate or in combination the process where a barrier layer is formed and the second semiconductor layer is formed over the barrier layer where a second heat treatment is used to getter the element to the second semiconductor layer and later removed the second semiconductor film.

15. All dependent claims are also rendered allowable.

16. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stanetta D. Isaac whose telephone number is 571-272-1671. The examiner can normally be reached on Monday-Friday 9:30am -6:30pm.

18. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on 571-272-1679. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

19. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Stanetta Isaac
Patent Examiner
April 9, 2004

John F. Niebling
Supervisory Patent Examiner
Technology Center 2800